IN THE CLAIMS:
Please amend the claims to read as follows:

1. (Currently amended) A computer system which includes a plurality of memory banks, comprising:

a processor unit which controls processing of an operation; and

additional processing units, each of which corresponds to one of the memory banks and performs the operation independently of the processor unit,

wherein the operation is performed by the additional processing units, using data stored in the corresponding memory banks, based on an instruction or data provided from the processor unit, said plurality of memory banks being external to said processing unit and external to said additional processing units.

2. (Previously presented) The computer system of claim 1, wherein the operation that each of the additional processing units performs includes at least one of calculating the data, reading the data from the memory bank, and writing the data to the memory bank.

3. (Previously presented) The computer system of claim 1, wherein an address of the data in the memory bank is provided by the processor unit, and each of the additional processing units reads the data by referring to the address and performs the operation designated by the processor using the read data, and writes a result of the process into the address.

4. (Previously presented) The computer system of claim 3, wherein, when the additional

processing unit receives information from the processor unit and the operation designated by the processor comprises one of four basic operations of arithmetic, the additional processing unit performs one of the four basic operations using the read data and the received information.

5. (Previously presented) The computer system of claim 3, further comprising at least one of:

an addition updating unit which updates the data located in the address designated by the processor unit to a value resulting from adding of the data and a predetermined value; and

a subtraction updating unit which updates the data located in the address designated by the processor unit to a value resulting from subtracting a predetermined value from the data.

6. (Original) The computer system of claim 1, wherein the processor unit performs a vector operation.

7. (Previously presented) The computer system of claim 1, wherein the processor unit comprises a plurality of processors, each of which performs an operation in parallel with another processor.

8. (Currently amended) A method of controlling computation in a computer system which includes a plurality of memory banks, said method comprising:

instructing, at a processor unit, additional processing units, each of which is connected to one of the memory banks and works independently of the processor unit, to perform an operation;

reading, at the additional processing unit, data located in an address designated by the processor unit from the corresponding memory bank;

performing, at the additional processing unit, the operation instructed by the processor unit using the read data; and

writing, at the additional processing unit, a result of the operation into the address designated by the processor unit,

wherein said memory banks are external to said processor unit and external to said additional processor units.

9. (Previously presented) The method of claim 8, further comprising:

receiving, at the additional processing unit, information from the processor unit, wherein the operation instructed comprises one of four basic operations of arithmetic, and the performing performs one of the four basic operations using the read data and the received information.

10. (Previously presented) The method of claim 9 comprising one of:

updating data located in the address designated by the processor unit to a value resulting from adding of the data and a predetermined value; and

updating data located in the address designated by the processor unit to a value resulting from subtracting a predetermined value from the data.

11. (Original) The method of claim 9, wherein the processor unit performs a vector operation.

12. (Previously presented) The method of claim 9, wherein the processor unit comprises a plurality of processors, each of which performs an operation process in parallel with another processor.

13. (Currently amended) A recording medium readable by a computer, tangibly embodying a program of instructions executable by the computer to perform a method of controlling computation in a computer system which includes a plurality of memory banks, the method comprising:

instructing, at a processor unit, additional processing units, each of which is connected to one of the memory banks and works independent of the processor unit, to perform an operation;

reading, at the additional processing unit, data located in an address designated by the processor unit from the corresponding memory bank;

performing, at the additional processing unit, the operation instructed by the processor unit using the read data; and

writing, at the additional processing unit, a result of the operation into the address designated by the processor unit,

wherein said plurality of memory banks are external to said processor unit and external to said additional processor units.

14. (Currently amended) A computer data signal embodied in a carrier wave and representing a sequence of instructions which, when executed by a processor, cause the processor to perform a method of controlling computation in a computer system which includes a plurality of memory banks, the method comprising:

instructing, at a processor unit, additional processing units, each of which is connected to one of the memory banks and works independent of the processor unit, to perform an operation;

reading, at the additional processing unit, data located in an address designated by the processor unit from the corresponding memory bank;

performing, at the additional processing unit, the operation instructed by the processor unit using the read data; and

writing, at the additional processing unit, a result of the operation into the address designated by the processor unit,

wherein said plurality of memory banks are external to said processor unit and external to said additional processor units.

15. (Previously presented) The computer system of claim 1, wherein each said additional processing unit locks out an access of its memory bank during a time the operation is being executed.

16. (Previously presented) The method of claim 8, further comprising:

locking out, at the additional processor unit, an access of the corresponding memory

bank to said processor during at least one of said reading, performing, and writing.

17. (Previously presented) The computer system of claim 1, further comprising:

a memory controller located between said processor unit and said memory banks, said memory controller controlling a transmission of instruction and data to said plurality of memory banks.

18. (Previously presented) The computer system of claim 17, further comprising:

an access arbitor located between said memory control unit and said additional processing unit to arbitrate exclusive control of a memory access to said memory bank.

19. (Previously presented) A parallel processing apparatus, comprising:

a processor unit which controls a processing of an operation;

at least one additional processing unit; and

a memory bank associated with each said at least one additional processing unit, each said memory bank being external to its associated processing unit and functioning independently of any other memory banks,

wherein:

each said memory bank is accessible by said processor unit to provide at least one of data and instructions to each said additional processing unit for said operation processing; and

each said additional processing unit can lock-out access to its associated memory bank during a processing of said operation.